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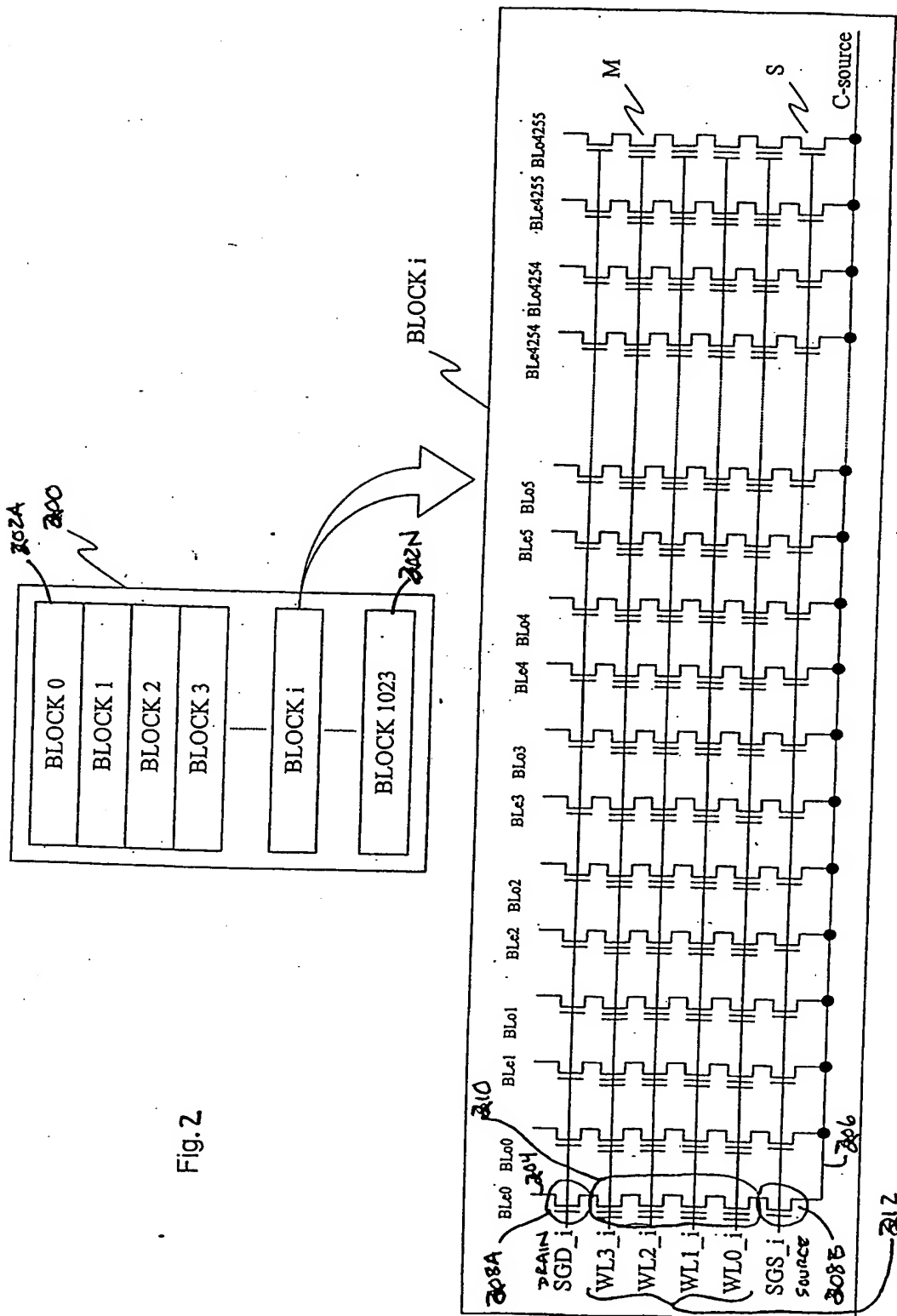


Fig. 2

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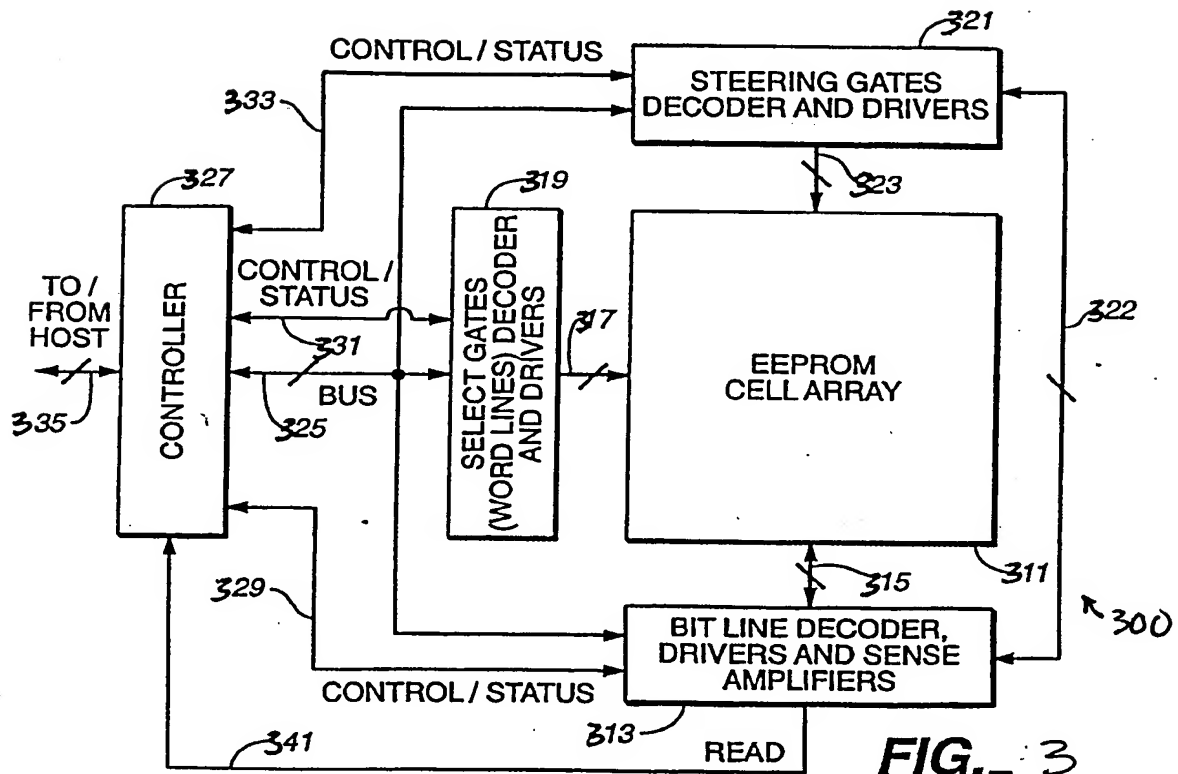


FIG. 3

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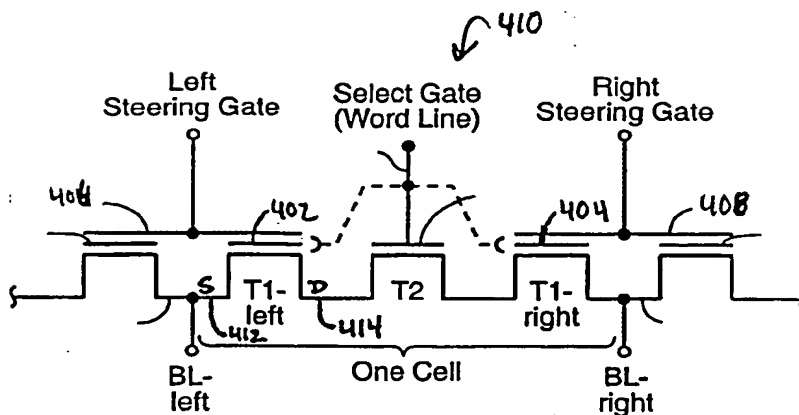


FIG. 4B

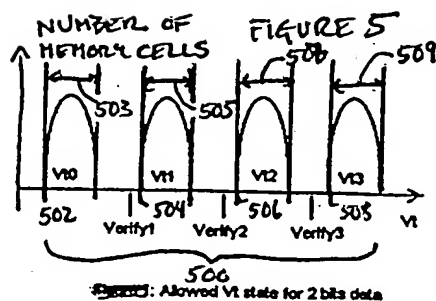


FIGURE 5: Allowed Vt state for 2 bits data

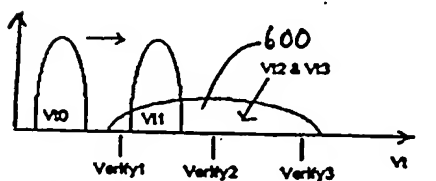


FIGURE 6: V12/V13 after Vt1 data complete Verity 1
Potential Problem with V2 cross Verity3 level

FIGURE 6

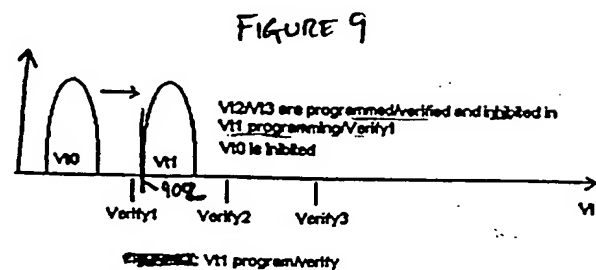


FIGURE 9

V12/V13 are programmed/verified and inhibited in
V11 programming/Verify1
V10 is inhibited

FIGURE 9: V11 program/Verify

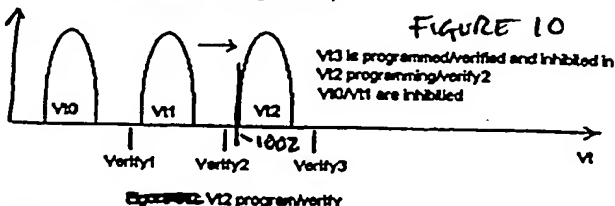


FIGURE 10

V13 is programmed/verified and inhibited in
V12 programming/Verify2
V10/V11 are inhibited

FIGURE 10: V12 program/Verify

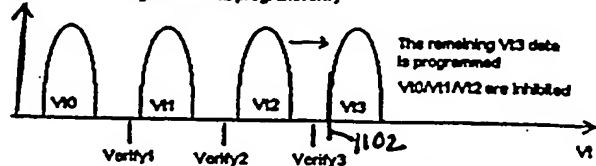


FIGURE 11

Figure 3.3: V13 program/Verify

FIGURE 11: Programming State Sequence of Suggested Algorithm

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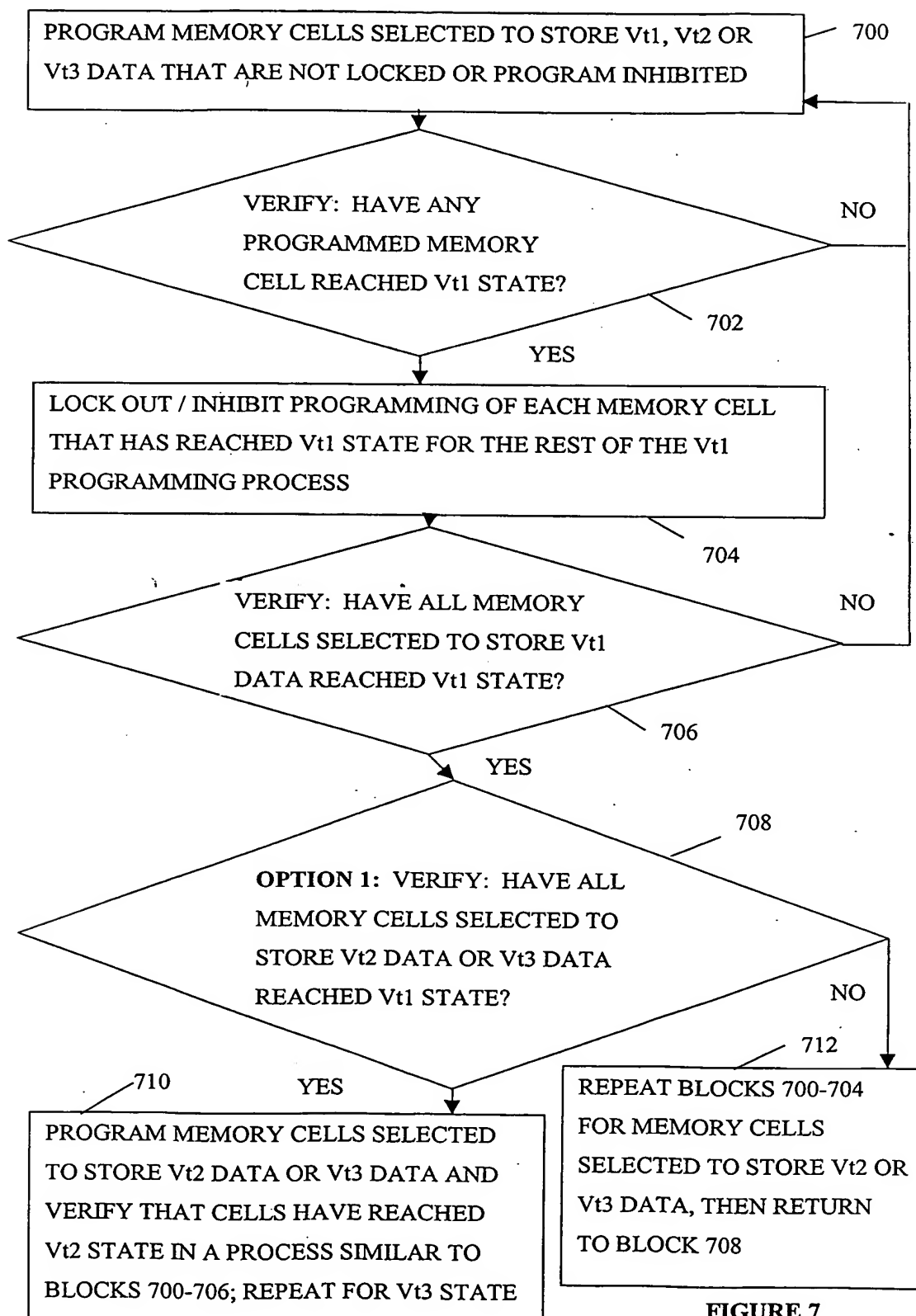


FIGURE 7

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FOI 64252001

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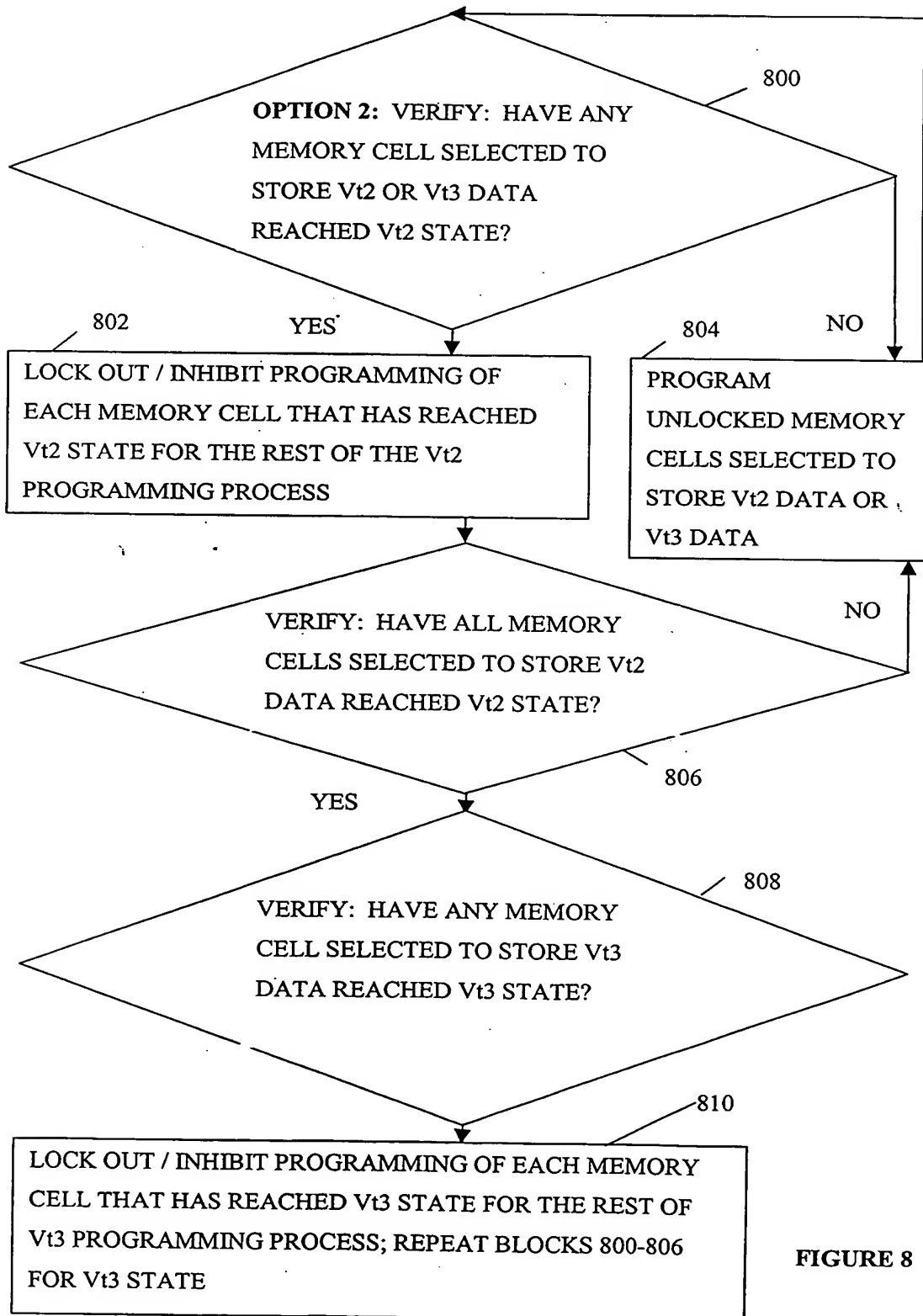


FIGURE 8

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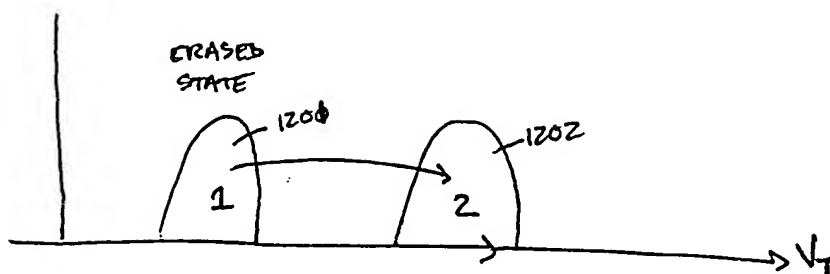


FIGURE 12 A

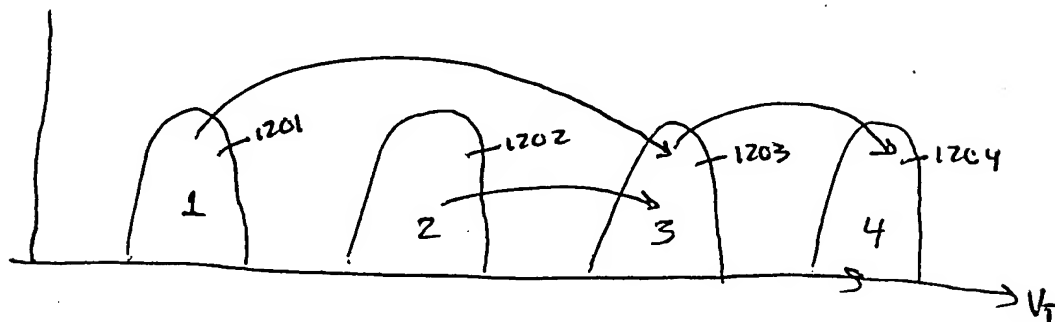


FIGURE 12B

10025749.121301